AlGaN/GaN HFET Including A Thin AlN Carrier Exclusion Layer

R S Balmer [1)] , D E J Soley [1)] , K P Hilton [1)] , K J Nash [1)] , M J Uren [1)] , A Wells [2)] , M Missous [2)] , T Martin [1)]

1) QinetiQ Ltd. St Andrews Rd, Malvern, Worcestershire, UK, WR14 3PS , 2) Dept. of Electrical Engineering and Electronics, UMIST, PO Box 88, Manchester, UK, M60 1QD

AlGaN/GaN microwave hetero−junction field effect transistors (HFETs) continue to produce impressive performance with power densities an order of magnitude higher than the equivalent GaAs device already achieved [1]. Previous theoretical studies have proposed the insertion of a thin AlN exclusion layer between the AlGaN barrier layer and the GaN buffer layer that will exclude carriers from the AlGaN layer and therefore minimise the alloy disorder scattering [2, 3]. A significant improvement in the mobility of the carriers in the 2D electron gas (2DEG) was predicted. Clear improvements in carrier mobility have indeed been demonstrated compared to conventional devices without the AlN exclusion layer [4−6]. Most noteworthy is for a silicon doped HEMT with a 1nm AlN exclusion layer which had a carrier density n_s=1.48×10^{13}cm^{-2} and room temperature mobility μ_{RT} =1542cm^{2}V^{-1}s^{-1} compared to n_s=1.1×10^{13}cm^{-2} and μ_{RT} =1200cm^{2}V^{-1}s^{-1} for a conventional device [5].

In this paper, we present a study of the effect of the insertion of a thin AlN exclusion layer in undoped HFET structures on sapphire and SI−SiC substrates. A dramatic improvement in carrier drift mobility is obtained from conductivity measurements on large devices when the exclusion layer is present. Capacitance−voltage analysis demonstrates that there is a larger effective band offset when there is an exclusion layer, and shows that reduced wavefunction into the barrier is expected, and hence improved mobility.

All HFET structures were grown by low pressure MOVPE using a Thomas Swan Close−Coupled Showerhead reactor and in situ optical monitoring described elsewhere [7]. After deposition of the nucleation layer on the substrate, an insulating 1.2µm GaN buffer layer was grown followed by a thin AlN and a 29nm $Al_xGa_{1-x}N$ layer (x=0.25). The AlN layer growth time was varied between 0 and 30secs to optimise the thickness. Each epilayer was measured using mercury probe CV to estimate the 2DEG carrier density and confirm buffer layer isolation, and by Lehighton contactless sheet resistivity mapping to give a rapid and non−destructive estimate of the channel conductivity [8]. Devices were fabricated using conventional mesa isolation, with TiAlAu source and drain ohmic contacts and NiAu gate contacts. Power transistors were passivated using silicon nitride.

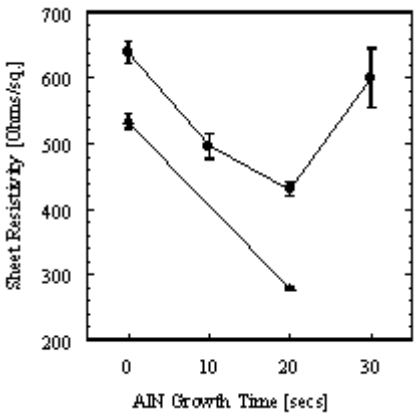


Fig. 1. A plot of mean sheet resistivity measured by Lehighton contactless resistivity mapper for a series of samples grown on sapphire (solid circles) and SI−SiC (solid triangles) with a AlN growth time of 0, 10, 20 and 30secs. Error bars refer to standard deviation from 55 point map.

Figure 1 is a plot of the mean sheet resistivity from a Lehighton map for a series of samples grown with an AlN layer growth time of 0, 10, 20 and 30secs. We found that the sheet resistivity varied significantly with AlN growth time giving a optimum of 430Ohms/sq. on sapphire and 280Ohms/sq. on SI−SiC for a growth time of 20secs. As the carrier density, n_s estimated from Hg−CV profiles was relatively insensitive to the AlN layer at about 1.0×10^{13}cm^{-2} (within the experiment error of ±10%), the large variation in sheet resistivity was almost entirely due to the channel mobility.

	Carrier Density, V_g=0V (10^{12} cm^{-2})	Sheet Resistivity (Ω/sq.)	Drift Mobility (cm^{2}V^{-1}s^{-1})
No AlN Layer	9.4	509	1308
AlN Layer	10.6	272	2177

Table 1. Zero bias drift mobility of devices from two representative samples on a SI−SiC substrate determined from separate carrier density and conductivity measurements.

The variation of drift mobility with sheet carrier density (i.e. versus gate voltage) was measured using large area (160×100μm) devices by separate measurements of electron density (capacitance voltage − CV) and conductivity (current voltage − IV) using a drain bias of 100mV [9] for samples with and without the optimum (20sec) AlN exclusion layer. The room temperature drift mobility for devices from two representative samples grown on SI−SiC at 0V gate bias was 2177cm^{2}V^{-1}s^{-1} and 1308cm^{2}V^{-1}s^{-1} respectively, see Table 1. Figure 2(a) is a plot of the drift mobility as a function of carrier density for the above samples. At low carrier concentrations both structures had comparable mobility. Without the exclusion layer the mobility dropped rapidly with increasing carrier density, but when the exclusion layer was inserted into the structure, the mobility was relatively independent of carrier density giving rise to the observed high mobility at zero gate bias.

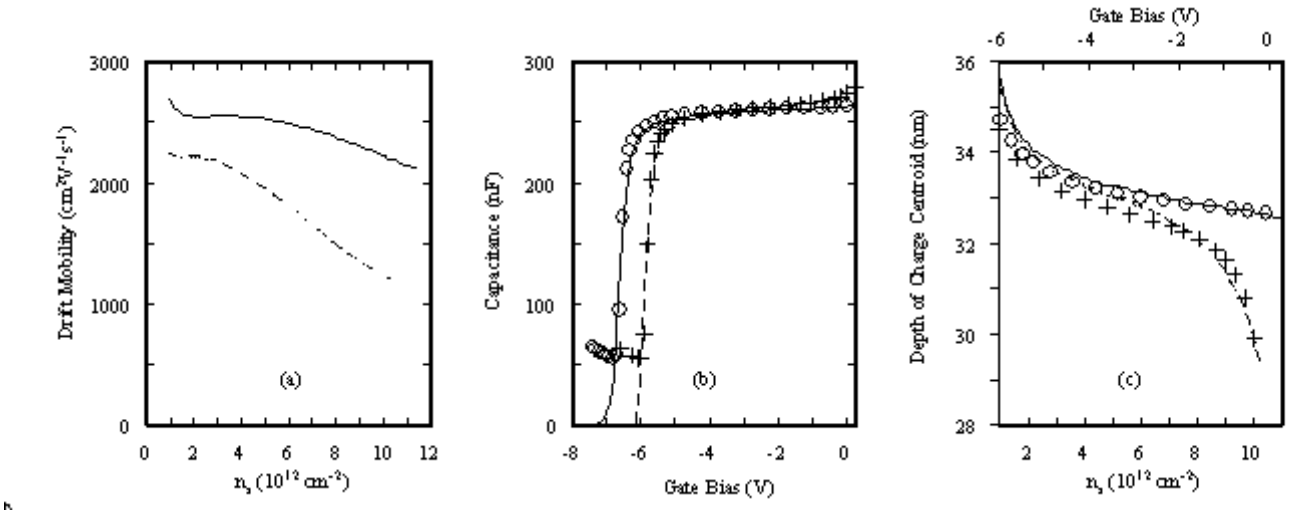


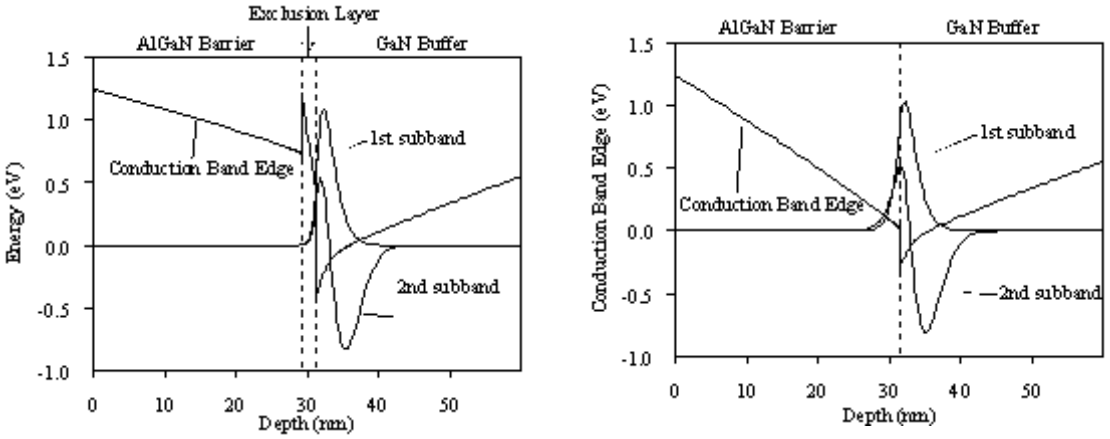
Fig. 2. (a) Drift mobility as a function of carrier density; (b) Capacitance as a function of gate voltage; (c) Location of the charge centroid as a function of carrier density. Experimental data is measured using large area (160×100μm) devices from samples grown on SI−SiC. Theoretical simulations were based on coupled 1D Schrödinger−Poisson calculations. Experimental data: with exclusion layer (solid line), without exclusion layer (dashed line); Simulated data: with exclusion layer (open circle), without exclusion layer (plus).

Figure 2(b) is a plot of the experimental CV data for samples with and without the optimum exclusion layer. The measured difference in the pinch−off voltage (0.75V) indicates that the aluminium concentration in the exclusion layer is less than that of AlN and rather is AlGaN with an alloy fraction x=0.592 [10].

The location of the charge centroid below the gate (depletion layer thickness as a function of carrier density) was calculated directly from the experimental CV data in fig. 2(b) assuming a parallel plate capacitor, and is plotted in fig. 2(c). When the exclusion layer is present, the 2DEG is constrained at a fixed depth, whereas in the absence of the exclusion layer the charge penetrates into the barrier layer at high carrier density.

Theoretical simulations of the CV data were performed using coupled 1D Schrödinger−Poisson calculations assuming abrupt interfaces and an exclusion layer thickness of 2nm, an example of which is shown in fig. 2(b). A deep level acceptor concentration was included in the GaN buffer as determined from substrate bias experiments [11]. The steep increase in capacitance when the bias voltage exceeds −2V observed with no exclusion layer, arises from the proximity of the AlGaN conduction band to the Fermi energy at low bias. This *turn−up* effect is absent

when the exclusion layer is present because the piezoelectric field in the exclusion layer increases the effective conduction−band offset, and raises the conduction band well above the Fermi energy at all reverse biases. To reproduce the turn−up effect in the simulations, donors were included in the AlGaN barrier layer with a binding energy of 0.2eV. The same number of acceptors were added, to maintain the value of $N_a-N_d=1\times10^{17}cm^{-3}$ throughout. Crude agreement of the calculated turn−up effect with experiment was found for $N_d=7\times10^{17}cm^{-3}$ and $N_a=8\times10^{17}cm^{-3}$.



(a). (b).

Fig. 3. Simulated band structure of AlGaN/GaN HFET (a) with and (b) without the exclusion layer based on coupled 1D Schrödinger−Poisson calculations. Included is the wavefunction for first and second subband to illustrate the penetration alloy.

The simulated band structure is plotted in fig. 3 (a) with and (b) without the exclusion layer. The barrier height preventing penetration of charge into the AlGaN barrier layer has increased from <100meV to just over 700meV as a result of the exclusion layer. Also plotted in fig. 3 is the calculated electron wavefunction (for clarity, only the first two subbands are plotted). The effect on the wavefunction penetration is dramatic with the presence of the exclusion layer. Considering the first subband only as this contributes the majority of the carriers (see Table 2); in fig. 3(b) the wavefunction decays relatively slowly in the AlGaN barrier layer with 13% of the wavefunction penetrating into the alloy compared to only 3% with the exclusion layer, which decays rapidly within the exclusion layer, fig. 3(a).

Table 2. The calculated relative scattering rate and sheet carrier density for each subband for zero bias on the device for the cases with and without the exclusion layer.

	With Exclusion Layer		No Exclusion Layer	
	L^{-1} (L^{-1} nm^{-1})	Density (10^{12} cm^{-2})	L^{-1} (L^{-1} nm^{-1})	Density (10^{12} cm^{-2})
Subband 1	1.09	9.862	6.58	8.436
Subband 2	0.207	0.540	2.24	0.491
Subband 3	0.142	0.031	3.01	0.034
Subband 4	0.122	0.003	10.2	0.004

The alloy scattering rate and its absolute contribution to the mobility cannot be calculated easily, but the factor that depends on wavefunction penetration into the barrier can be calculated easily. This relative scattering rate is an inverse length, and allows simple comparison of different cases.

Table 2 presents this relative scattering rate for intra−subband scattering, together with the sheet carrier density

for each subband for zero bias on the device. The relative scattering rate in the first subband is a factor of six higher in the case with no exclusion layer than in the structure where the exclusion layer is present, hence the improved mobility observed in fig. 2(a).

Interestingly, although very high performance transistors have been demonstrated using the AlN layer, there has not been an obvious improvement in small signal performance seen compared to conventional designs [5, 6]. Consistent with this observation, our 2×50μm devices with and without the exclusion layer showed similar small signal RF performance of f_T ~33GHz and f_{MAX} ~80−100GHz for a 0.25μm gate. To explain this observation, we note that the maximum f_T is obtained at a gate voltage close to pinch−off with low carrier density (a class AB or class B operating point). As shown in fig. 2(a), the small signal mobility at that bias point would be comparable for both devices. Of course, at high fields and under realistic operating conditions the situation is complicated by real space transfer (RST) where hot electrons spill over into the AlGaN layer from the 2DEG potentially reducing the mobility and the saturated velocity. Also, source resistance is different in the two cases, and does have a second order effect on f_T [12]. The benefits of including the exclusion layer may well be reduced source resistance and potentially linearity [2].

In conclusion, we present a study of the effect of the insertion of a thin exclusion layer in undoped HFET structures. A dramatic improvement in room temperature carrier drift mobility is observed with a value of $2177 cm^2V^{-1}s^{-1}$ obtained for an optimum growth time of 20secs on a SI−SiC substrate. Furthermore, electronic structure calculations characterise the exclusion layer from its measured effect on the pinch−off voltage, and show that there is a larger effective band offset when there is an exclusion layer (fig. 2 (a) and (b)). The calculations find that this increased band offset has two effects: it eliminates the steep increase in capacitance when the bias voltage exceeds −2V observed with no exclusion layer by raising donor states in the AlGaN far above the Fermi energy; and it greatly reduces penetration of the subband wavefunctions into the AlGaN, thereby reducing alloy scattering in the channel and improving the mobility.

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